*The Good Ol’ Game of Checkers*

*(VERILOG Edition)*

**Verilog Designers:** Anikeith Bankar & Brendan Leder (Station #61)

**Project Name:** Checkers board game in Verilog with VGA Monitor support.

**Scope of Project:** We decided to turn the boring old game of checkers and turn it into a full DE1-SOC FPGA supported version of the board game. Setting up the physical board with so many little pieces and keeping track of your pieces are keeping millions of players from enjoying their game of Checkers a lot sooner. The inputs from the FPGA will simulate the Checkers pieces moving throughout the game and the simulation will be shown on the monitor.

**Design of the Game:**

1. Setting up the state of the board
   1. We will be using a 8x8 board that will be pre-set with two colours (one on each side). The columns of the simulated board will be toggled with the SWITCHES on the FPGA board. The keys on the FPGA board will allow the user to switch between their own pieces in that column specific to their own colour.
   2. The graphics of the game will be made using the VGA adapter modules.
2. Functionality of the game
   1. The KEY inputs on the FPGA board will allow the user to make a straight vs. right diagonal vs. left diagonal moves on the game board with support of the aforementioned input of toggling between checker pieces. The number of steps forward the user decides to move is also decided with key input from the FPGA board.
3. Keeping Track of Score
   1. The HEX displays on the board will keep track of the score between the two players.
4. Winner!
   1. The LEDRs on the FPGA will start to flow in the right direction for player 1 win or will start to flow in the left direction for player 2 win. This will be supported with a HEX display showing the player who won as well.
5. End of Game
   1. There will either be a natural winner of the game or a specific time limit is reached, and the game terminates with the player with the most pieces of the opponent’s pieces winning the game. To make the game more exciting, when the game is down to the last 8 pieces on either side, the user will only have 5 seconds to make their move or the turn changes automatically. To quit game abruptly, a KEY will be used to reset game.

**Checkers Game Block Diagram (VERILOG)**

**Milestones**

1. Week 1: Function checkers game in VERILOG using the input switches is completed
2. Week 2: The display for the game is complete
3. Demo Day: Connected Verilog checkers game with the display with full functionality as above